

Applicants respectfully disagree and traverse the above rejections as set forth below. Independent claim 1 is not anticipated by and is allowable over Yu for at least the reasons that Yu failed to teach, suggest or disclose every features of the claimed invention. More specifically, Yu failed to teach, suggest or disclose at least "an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, whereby an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing latch-up of the ESD protection circuit", as required by claim 1. The technical impact of connecting the anti-latch up circuit between the voltage source Vcc, the SCR circuit, and the GND is that this will allow node A of the anti-latch up circuit to maintain a voltage equivalent to the voltage source Vcc, thus, the SCR circuit of the claimed invention will not be unexpectedly activated. In case of an ESD event (due to positive current) the voltage level on the node A cannot race the rising rate of the voltage source Vcc because the rising time of the ESD event is much shorter than the rising time of the RC circuit, thus the SCR circuit will trigger normally. Thus the internal circuit is protected from an ESD damage.

The Office Action recognized that Yu failed to disclose a voltage source, but asserts that this feature is inherent in Yu's device as the line connecting the pad and the internal circuit is the voltage source. Applicants would like to particularly point out that like the conventional ESD protection circuit design, Yu discloses an ESD protection circuit design. Substantially, Yu discloses an EPROM and a SRC circuit connected between the I/O pad and the internal circuit (please see col. 5, lines 45-50). According to Yu, in an ESD event the EPROM enters breakdown and triggers the SCR to operate in the snapback region for bypassing the ESD stress in order to prevent the internal circuit from ESD damage. It is clear that the EPROM of Yu does not function like the anti-latch up circuit of the claimed invention. The EPROM of Yu is substantially for activating the SCR circuit while the anti-latch up of the claimed invention is designed for preventing the SCR circuit from being unexpectedly activated.

Therefore, Yu failed to teach, suggest or disclose an ESD protection device comprising "an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, whereby an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing latch-up of the ESD protection circuit", as required by claim 1. Accordingly, Applicants respectfully submit that Yu cannot possibly anticipate claim 1 in this regard.

Further, because the anti-latch-up circuit of the claimed invention is connected between the voltage source and the GND, as claimed in claim 1, and since the voltage source is shared by a plurality of pads, this circuit design allows the use of only one anti-latch-up circuit for many pads. Therefore, the space occupation can be substantially reduced thereby increasing the integration of the device. To the contrary, Yu's RC circuit is coupled between the pad and GND, therefore, Yu's circuit design requires one RC circuit for each pad. Accordingly, Applicants respectfully submit that Yu cannot meet the claimed invention in this regard.

For at least the foregoing reason, Applicants respectfully submit that claim 1 and its dependent claims 3 and 4 are not anticipated by Yu and patently define over Yu. Reconsideration and withdrawal of these rejections is respectfully requested.

Response to Rejections under 35 U. S. C. 103

2. The Office Action rejected claim 2 under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Ker et al. (US-5,754,380, hereinafter Ker).

In rejecting the above claims, the Office Action asserted that Yu teaches substantially the entire claimed structure, as applied to claim 1 above, except a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source. Ker et al. in FIG. 1, teaches a first diode 70, having a first input end and a second diode 60, having a first input end and a second input end, respectively connected to the I/O pad and a

voltage source. It would have been obvious to a person skilled in the art at the time of the invention to use a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end, and a second input end, respectively connected to the I/O pad and voltage source in Yu's device in order to provide better protection for the device against ESD event.

Applicants respectfully disagree and would like to particularly point out that since claim 2 depend from independent claim 1, and since independent claim 1 is allowable over Yu for reasons set forth in paragraph 1 above, claim 2 also patently defines over Yu for at least the same reasons. Further, because the Office Action relied upon Ker for showing a first diode and a second diode, still Ker cannot cure the specific deficiencies of Yu. Accordingly, Applicants respectfully submit that claim 2 patently defines over Yu and Ker. Reconsideration and withdrawal of these rejections is respectfully requested.

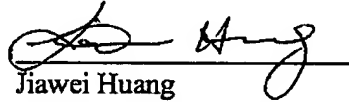
CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-4 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Date: 6/5/2002

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809

Respectfully submitted,
J.C. PATENTS


Jiawei Huang
Registration No. 43,330

FAX COPY RECEIVED

JUN 05 2002